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U.S.S.N.: 10/731,622
Filing Date: December 9, 2003
EMC Docket No.: EMC-01-102CIP1

Amendments To The Specification:

Please change the title of the application to the following:

--DATA STORAGE DEVICE WITH TWO-TIER RAID CONTROL CIRCUITRY--

Please replace the paragraph beginning on page 1, line 4 with the following:

This application is a Continuation-in-Part of U.S. Application Serial No. 10/004,090, now U.S. Patent No 7,174,422, entitled Data Storage Device with Two-Tier Raid Control Circuitry, filed October 3, 2001.

Please replace the paragraph beginning on page 10, line 1 with the words “Despite conventional.. “, and ending on page 10 line 14 with the words “... in greater detail.” with the following:

Despite conventional wisdom that holds high speed memory chip caches should be used to mask the slower speed of disk based data storage, using device 106 in a cache 132 can offer a number of potential advantages over memory chips. For example, as disks retain their contents absent power, the device 106 can offer greater data protection in the event of a power failure. The device 104 can also potentially enlarge the storage capacity of a cache. Additionally, depending on its configuration, the device 104 may also offer better thermal, power, and data density characteristics. Further, in the current marketplace, the device 106 may reduce the cost of a cache 132 relative to a memory chip implementation. Co-pending U.S. Application Serial No. 10/001,317, now U.S. Patent No. 6,973,537, entitled “Disk Cache Interfacing System and Method”, describes such a cache in greater detail.